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IP in Design

Case studies in Design Re-use

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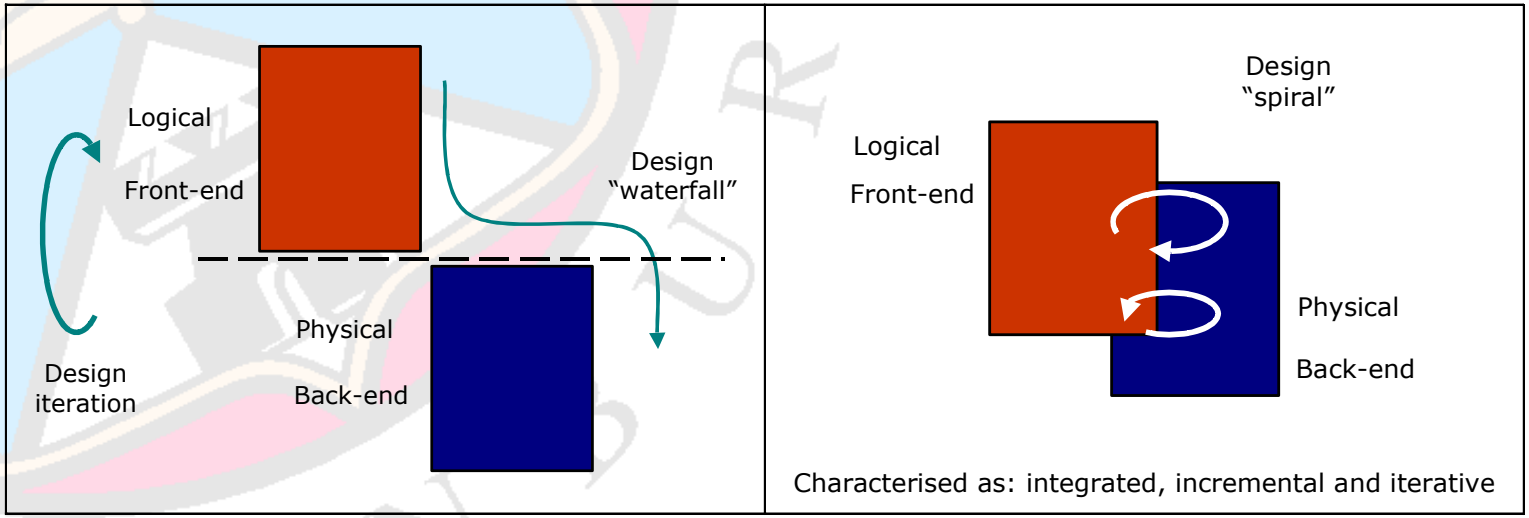
ASIC vs DSM Flows



The most common manifestation of the failure of both flows is in inability to achieve timing convergence: chips cannot be designed to satisfy their timing constraints and multiple design iterations between logical and physical design do not resolve timing problems

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Re-Use

- The amount of resources and time allocated to new SoC designs does not scale with the complexity of the systems being developed.
- Levels of Re-use >90% are required.

Socketisation

Why?

- Allow for multiple use
- Compliance with standards
- Enhancement

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Overheads?

"Designing a function block for true re-usability is exponentially more difficult than building a function block for one use only"

Philips

Impacts:

- Design Analysis
- Verification
- Documentation

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Main activity

- Prototyping High Performance IP cores.
- Platform design.
- Integration Schemes.
- Reconfigurable Low Power Hardware

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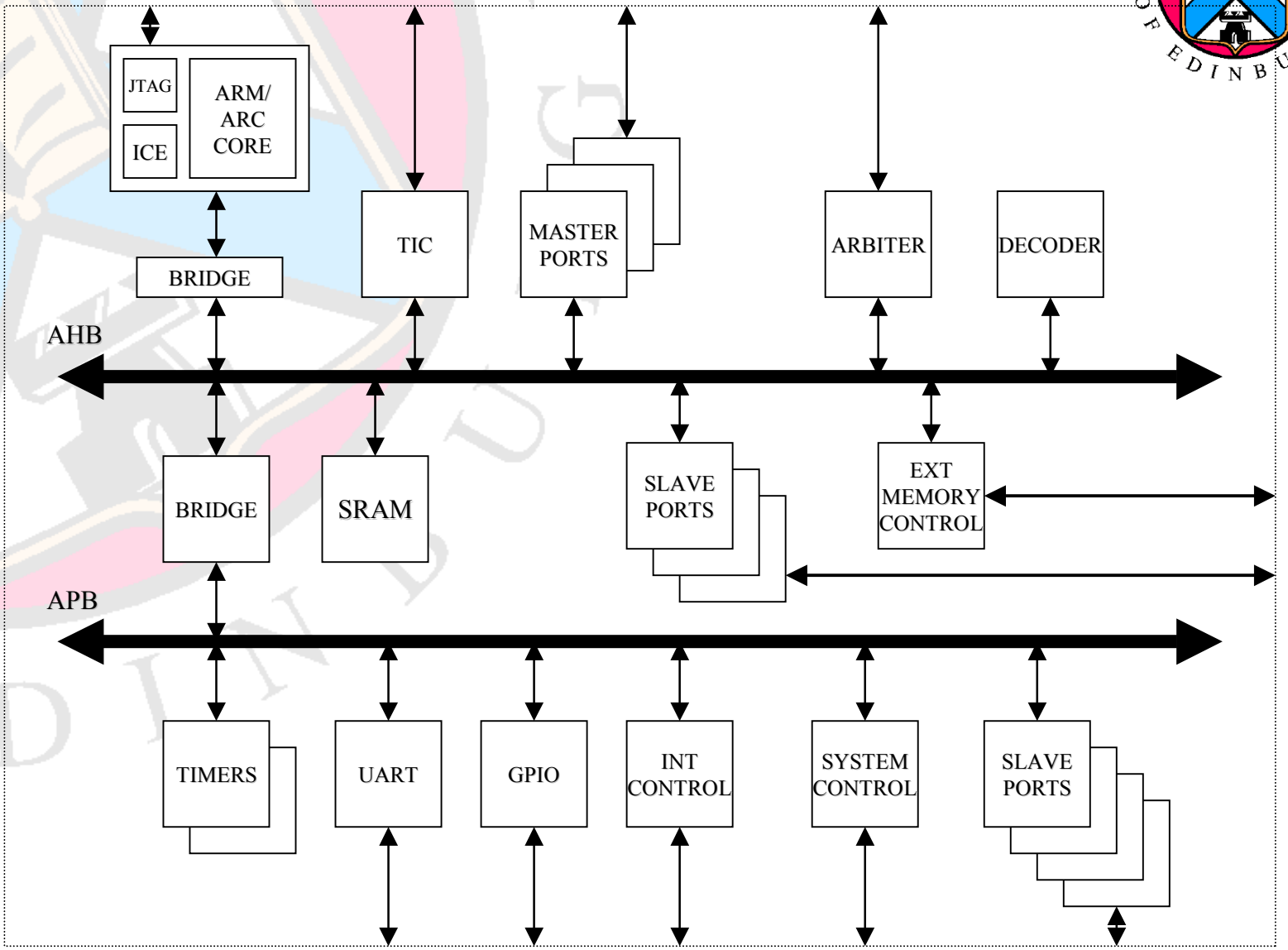
SoC Platform Design



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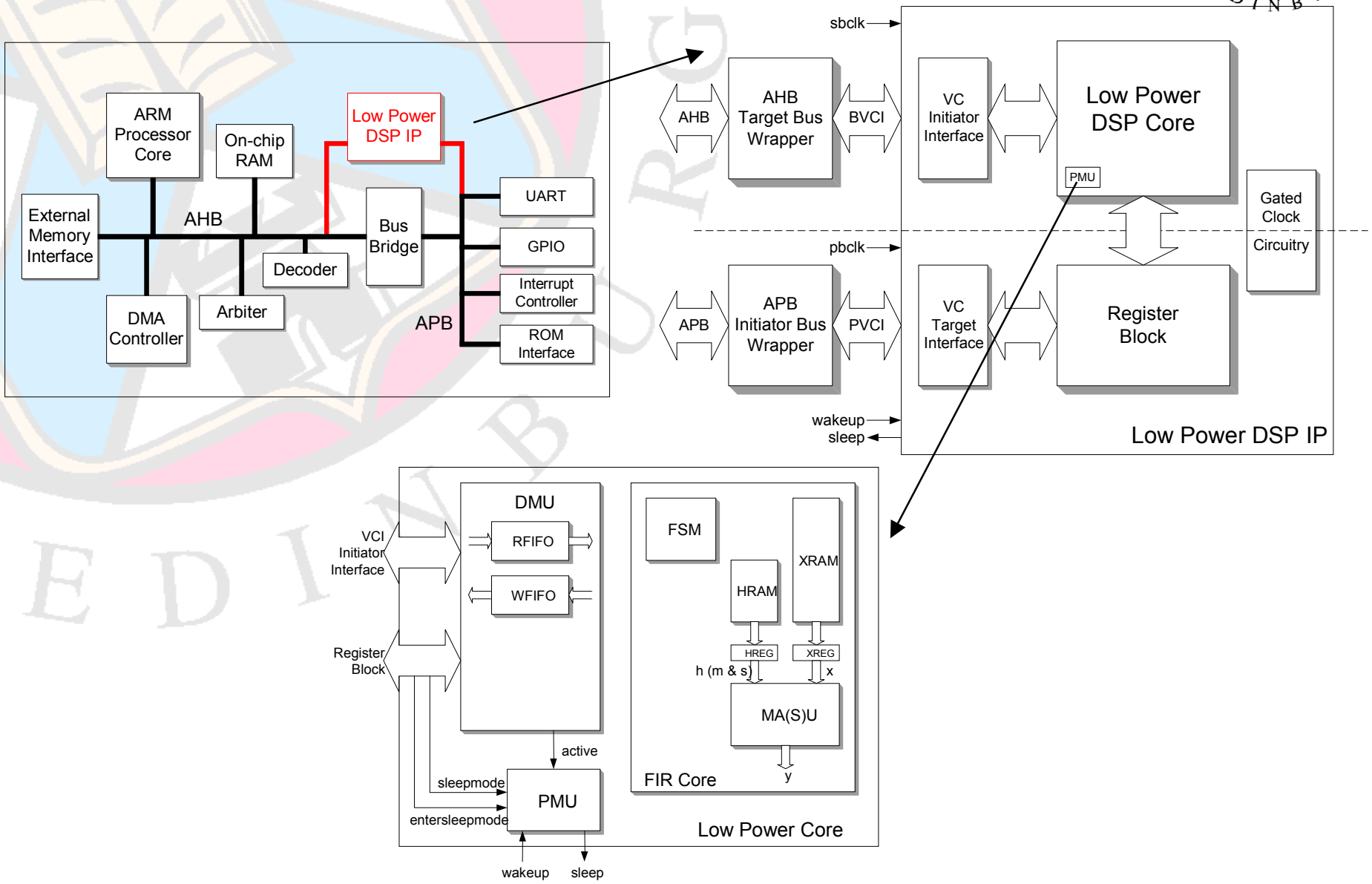
Platform Design & Interfacing

Epson + Motorola



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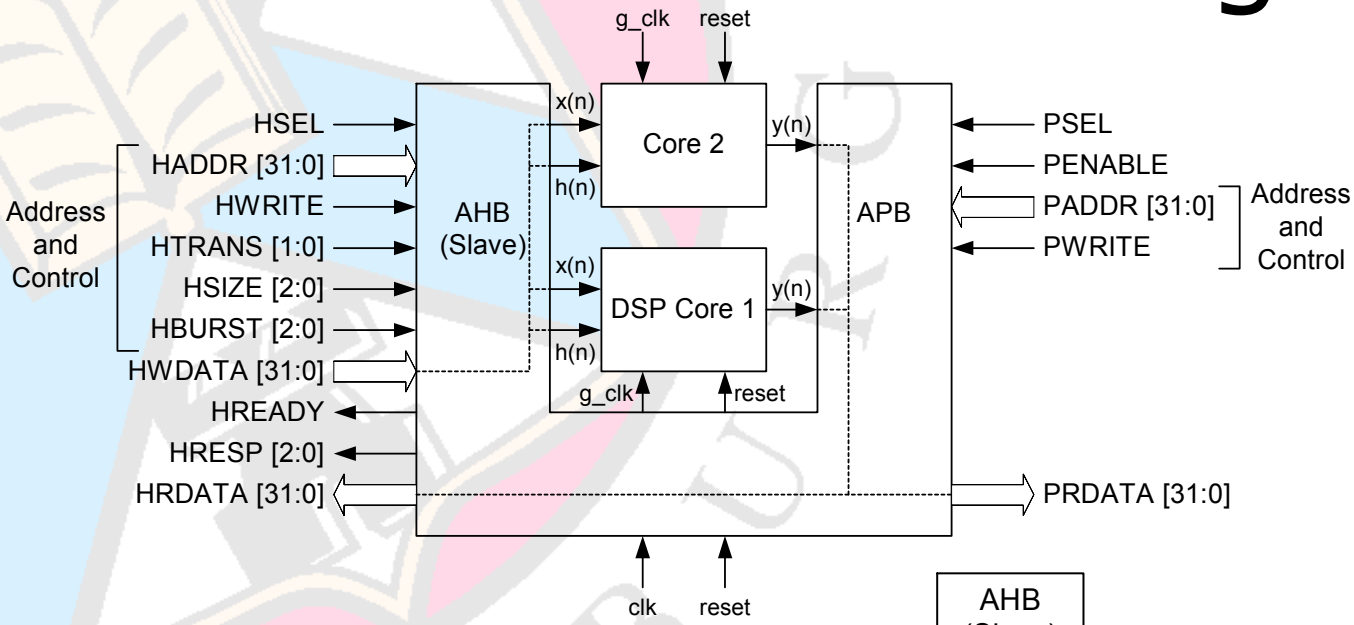
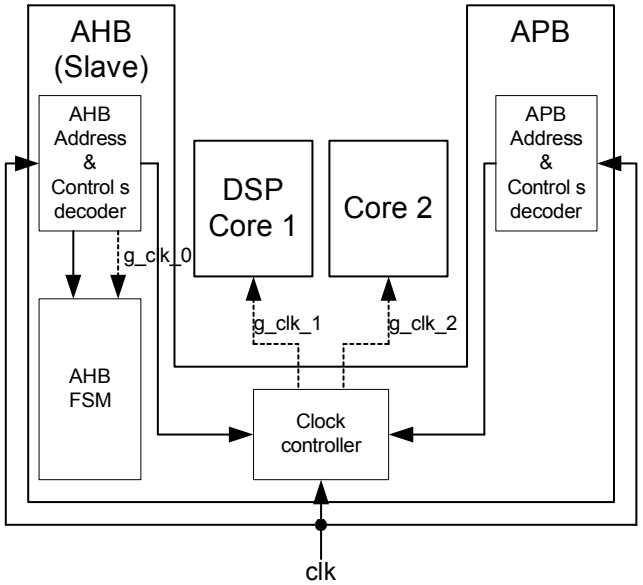
SoC Interfacing





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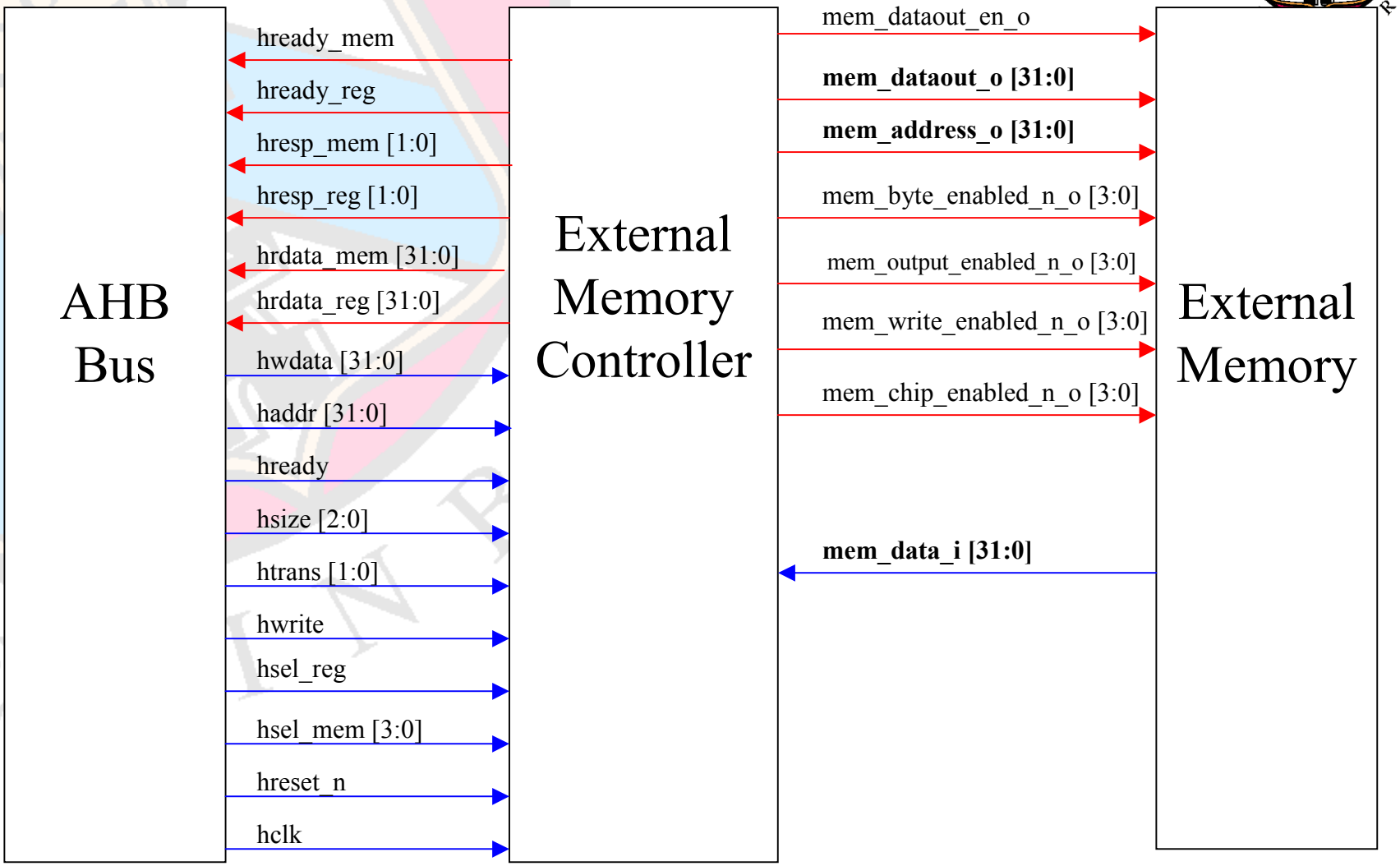
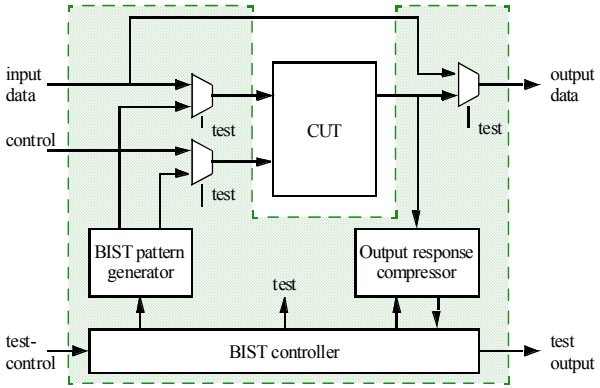
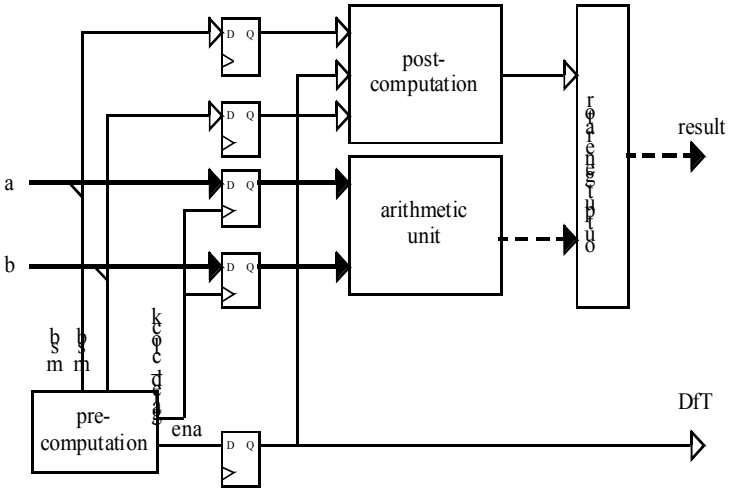
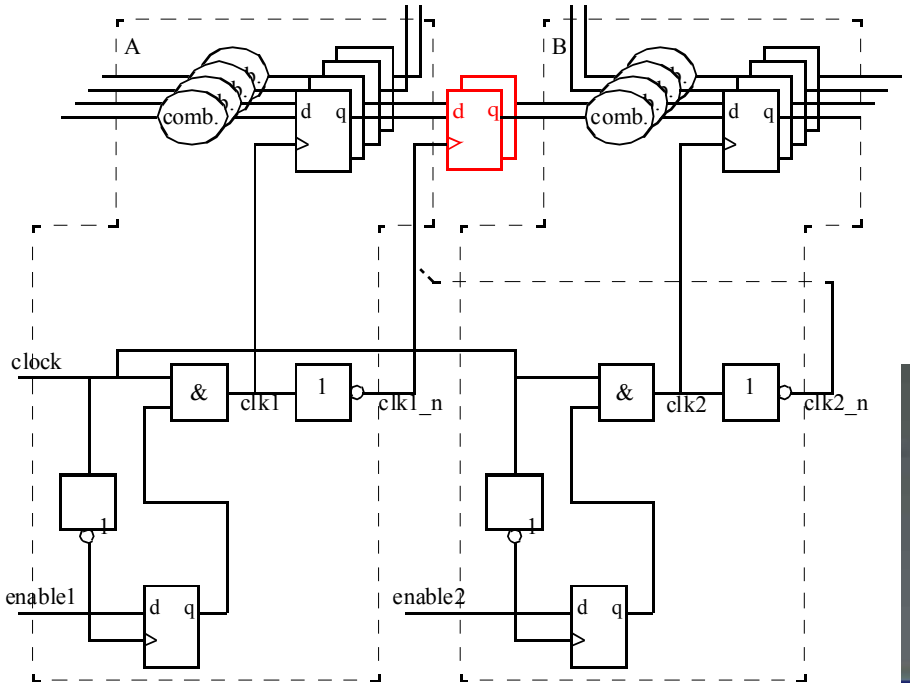
Low Power memory Control for an ARM based Platform (Motorola)



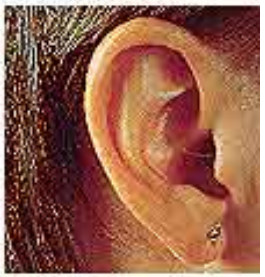
CIC hearing aid and Macro IP Shells
Bernafon (Switzerland)







1V power supply
30 mm^3 volume
70 mAh battery capacity
50+ hours operation



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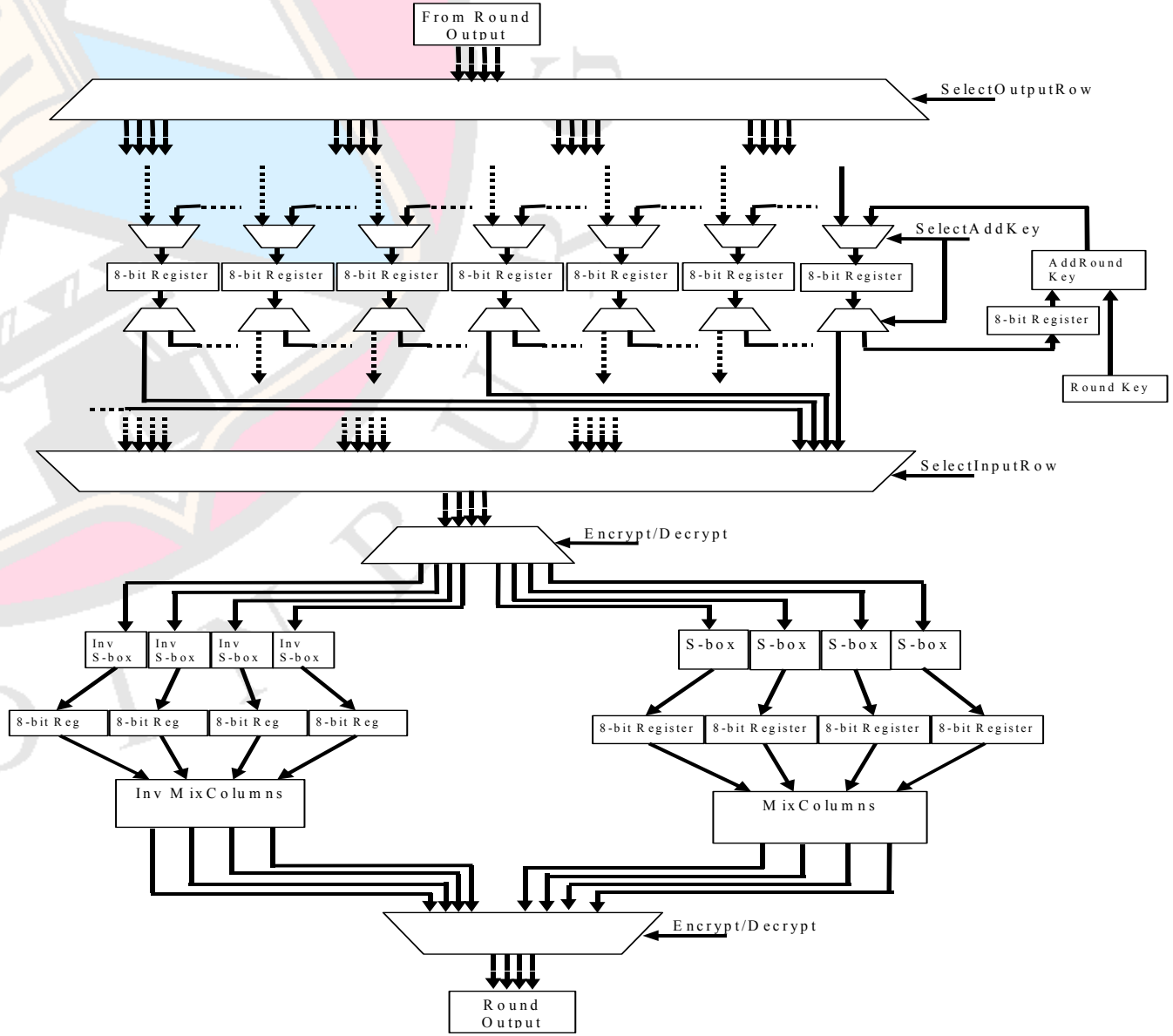
AES & RSA Encryption IP Cores - ATMEL



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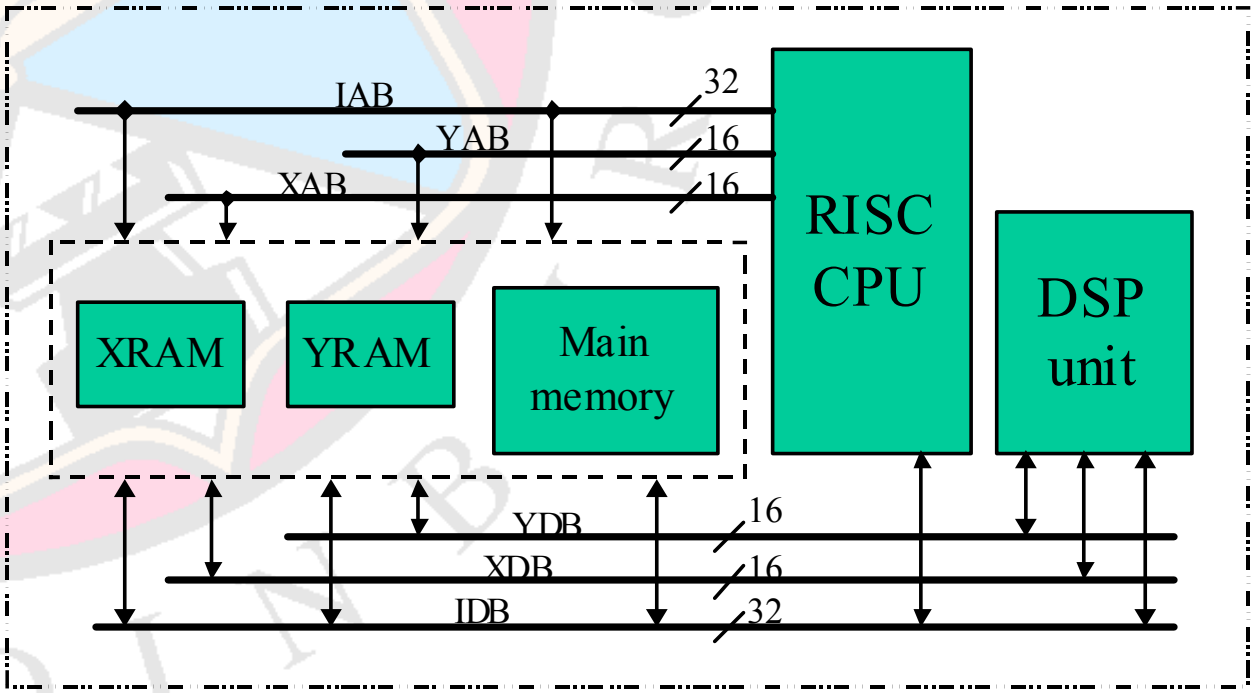
HITACHI Inspire the Next

Heterogeneous systems



- Changing system parameters
- Prediction of behaviour

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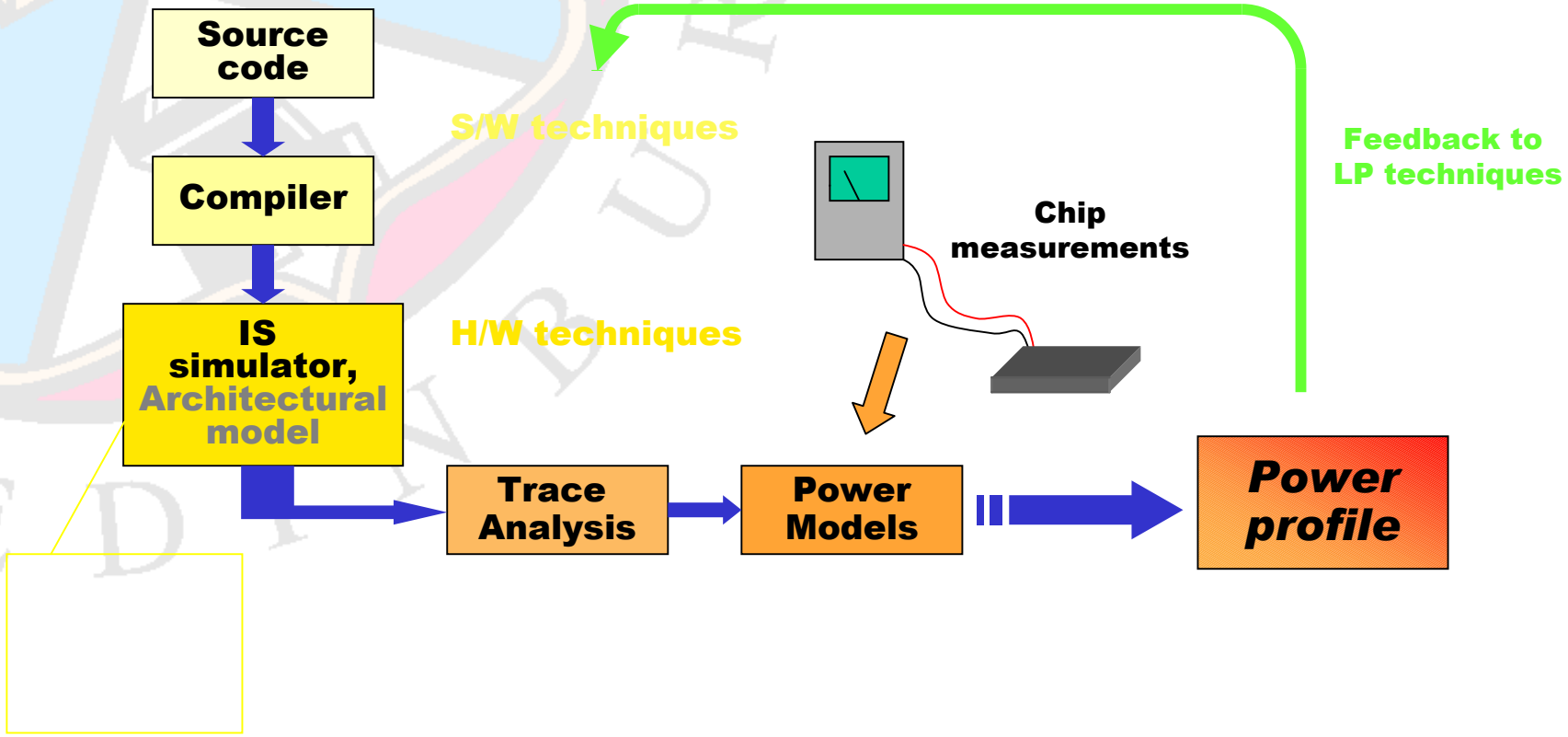
Evaluation of Embedded S/W and H/W Blocks for Smart Cards GSM Phones



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IP Cores

- FIR Filters
- DCT
- Wavelets
- FFT
- Encryption
- Memory Controllers
- CDMA

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Parameterisation Options

IPs	*wordlength*	*Filter order*	*Internal accuracy*	*Multiplier type*	*Number of multipliers*	*Data representation*	*Filter type*	*Block size*	*Ordering algorithm*	*Segmentation algorithm*
IP1	√	√	√	√	√	√	√	-	-	-
IP2	√	√	√	√	√	√	√	-	-	-
IP3	√	√	√	√	√	√	√	-	√	-
IP4	√	√	√	√	√	√	√	√	-	-
IP5	√	√	√	√	√	√	√	-	-	√
IP6	√	-	√	√	√	√	-	-	√	√

where

Multiplier type: Booth, Baugh-Wooley, Wallace, Dadda, etc.

Data representation: Two's complement, sign-magnitude, mixed, etc.

Filter type: Symmetric, antisymmetric, unsymmetric.

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Epson Scotland

- SoC Platforms and Design Methodologies for Speech Coding (EngD).
- Reconfigurable SoC Platforms for MPEG4 (PhD)