

# Jennic

TECHNOLOGY FOR A CHANGING WORLD

## ***The Case for Outsourcing Silicon Engineering***

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# Company Overview

- Privately owned Sheffield based company, Est. 1996
- Secure financial backing
- 50 employees, 40+ engineers
- Over a dozen tier 1 customers
- Established system-level IP portfolio
- Established design service capability
- Track record of right-first-time silicon
- Profitable despite difficult market conditions

***“A leading provider of system level Intellectual Property and Silicon Design Services to the broadband communications market.”***



# Creating Production Quality Silicon

## Some Issues...

- **System Architecting and Partitioning**
  - Hardware vs Software – Flexibility
  - Adherence to standards?
- **FPGA vs ASIC implementation**
- **Time to Market**
- **IP Design, Acquisition and Integration?**
- **Mixed Signal requirements?**
- **Reference boards and software drivers**
- **Understanding what's possible**



# Potential Silicon Solutions

## FPGA vs ASIC Comparison

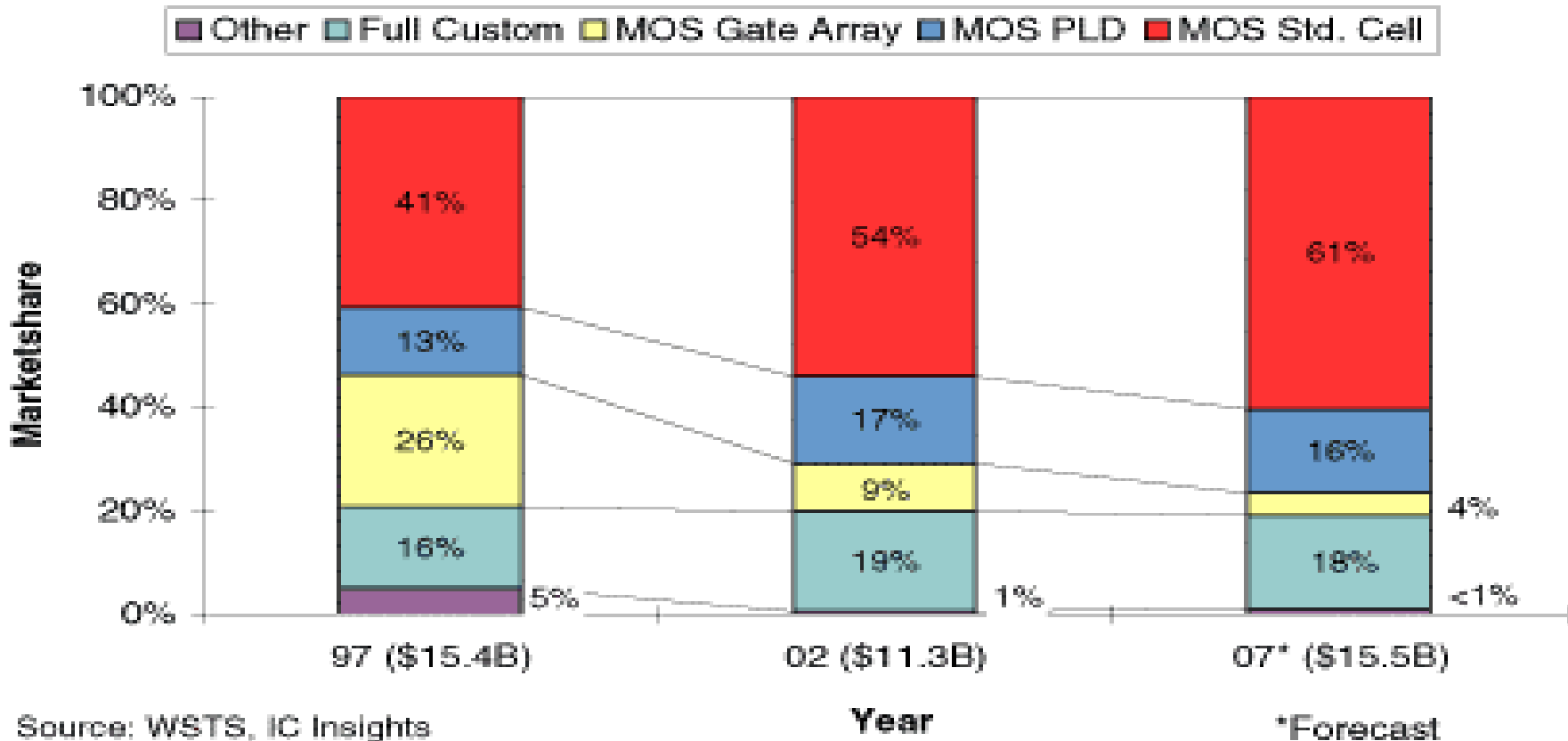
	Initial Cost (NRE)	Per Piece Cost	Density	Performance	Time to Market	Re-Spin Cost
<b>FPGA</b>	Low	High	Low	Low	Fast	Low
<b>ASIC</b>	High	Low	High	High	Slow	High

## Economic Pressures

Product Volume	Market Force		
	Price	Performance	Time to Market
High	ASIC	ASIC	FPGA
Low	FPGA	ASIC	FPGA



# ASIC Product Segment Market Share



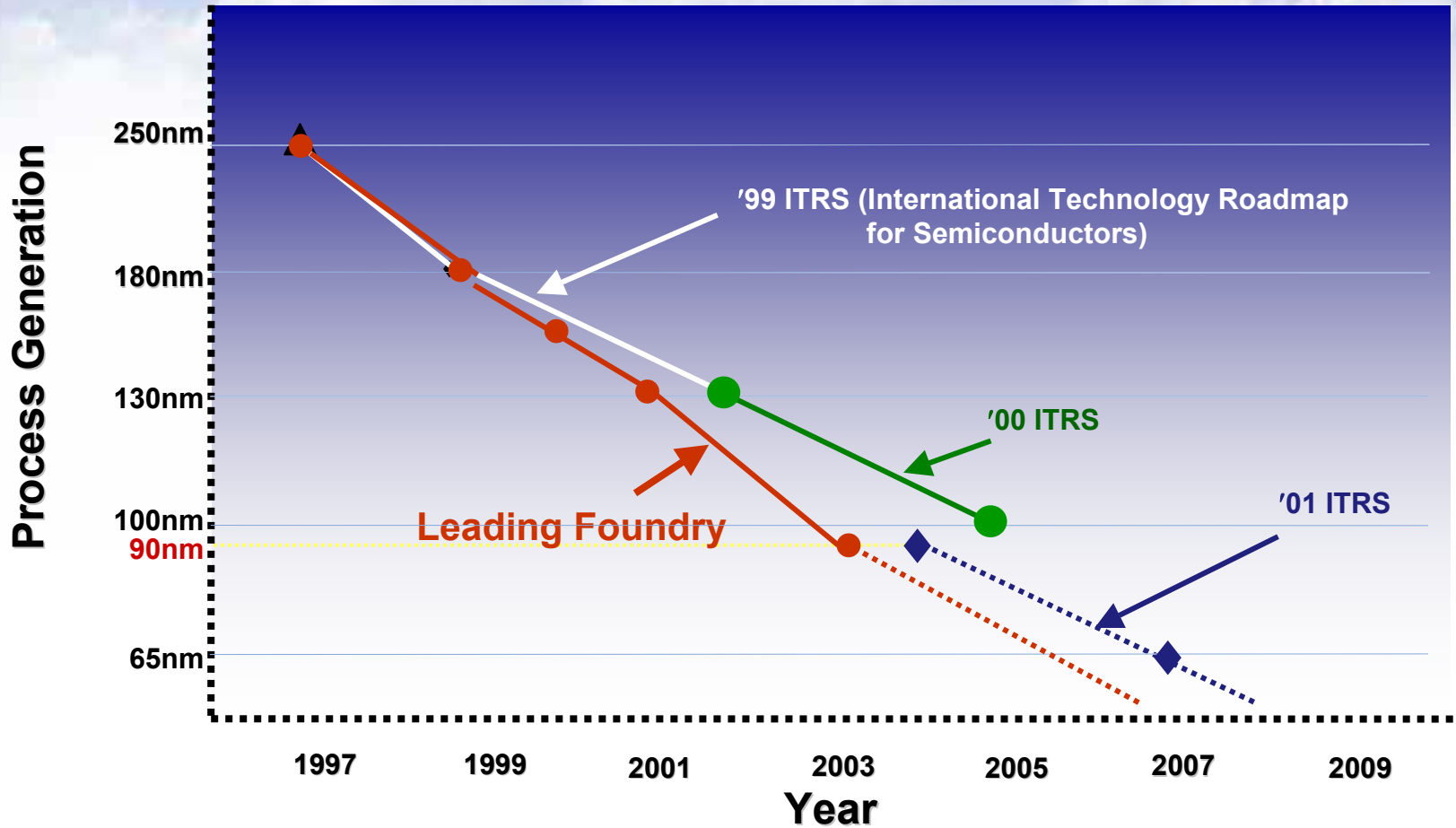
Source: WSTS, IC Insights

Year

\*Forecast



# Technology Trends



# ASIC Integration Potential

<b>Technology</b>	<b>250nm</b>	<b>180nm</b>	<b>130nm</b>	<b>90nm</b>
<b>Gate Density</b>	50K/mm <sup>2</sup>	100K/mm <sup>2</sup>	200K/mm <sup>2</sup>	400K/mm <sup>2</sup>
<b>Approx. usable gates</b>	5-10m	10-20m	20-40m	40-80m
<b>Interconnect Layers</b>	4 (Al)	6 (Al)	9 (Cu)	9 (Cu)
<b>Typ. Operating Voltage</b>	3.3V	1.8V	1.5V	1.0V
<b>I/O freq. (max)</b>	155MHz	622MHz	3.125GHz	5GHz??



# ASIC Implementation Overview

**Specification**

**Partition System – develop detailed device description.**

**Chip Design**

**Hardware/Software Tradeoffs. Identify IP Requirements  
RTL Coding. MS Design**

**Verification**

**Validate that design meets functional requirements.**

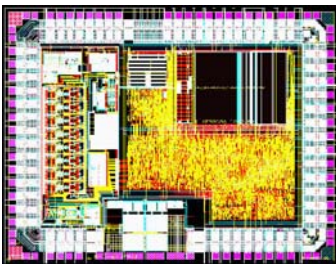
**Physical Implementation**

**Realise design database in target technology.  
Complete design closure; timing, power, SI**

**Sign Off**

**Verify that physical database meets technology design rules  
and is equivalent to design database**

**GDSII**



# ASIC Implementation – Major Risk Factors

- **IP Identification & qualification**
  - **Quality** : Has the IP been proven in silicon? Can it be easily tested?
  - **Support** : Does the vendor have a proven track record. Documentation?
  - **Cost** : Can the value of the IP justify its cost?
- **Functional Verification**
  - “Proving” large complex designs meet specification is both time consuming & costly – up to 40% of total project cost
  - **Culture Shift** – “Design Engineers” & “Verification Engineers”
  - **Estimated that 80% of 130nm designs integrate one or more processors**
  - **Estimate that by 2006 75% of all ASIC designs will have MS content**
- **Physical Implementation**
  - **Circuit delays dominated by interconnect**
  - **Deep sub-micron issues such as SI, IR drop, EM must be accounted for**
  - **Large databases mandate hierarchical methods**
  - **Integration of mixed signal IP requires special care**



# ASIC Implementation

## Identifying Key Skill Sets

- **Experienced Engineering Skills Needed in**
  - Silicon system architecting and partitioning
  - IP design, acquisition and Integration
  - Mixed signal design
  - Systems-on-Chip Engineering
  - Synthesis, Test, Layout, Digital/Mixed-Signal Integration
  - Supplier management
  - Reference boards and software device drivers
- **Also Costly in terms of**
  - Capex cost of EDA Tooling and Infrastructure
  - Management time in building and running a team
  - Management time in supplier relationships
- **Use of ASIC Vendors can cut some of these costs but...**



# ASIC Implementation - The Choices

- **ASIC Vendor**

- **Pros**

- IP licencing agreements for key IP (eg ARM)
- Handle design implementation from RTL/netlist
- Deliver packaged tested samples
- Handle yield issues & supply chain management

- **Cons**

- Limited IP portfolio
- High NRE
- Higher part price

## Foundry (Fabless)

- **Pros**

- Lowest NRE
- Lowest part price
- Widest selection of 3<sup>rd</sup> party IP

- **Cons**

- Design implementation & test provision
- Responsibility for packaging & test specialists
- Responsibility for yield issues & supply chain management



# ASIC Implementation

## The Outsourced Solution

- **Select “Best in Class” to provide required services**
  - **IP Solutions**
  - **Custom Mixed Signal Design**
  - **Physical Implementation**
  - **Pure-Play Foundry/ASIC Vendor**
  - **Packaging House**
  - **Test House**
- **Advantages**
  - **Minimise capital expenditure**
    - **EDA Tooling**
    - **IT**
  - **Minimise management overhead**
  - **Expand & complement existing teams in system expertise**



# Selecting Outsourcing Partners

- **Competent Design Service Provider should**
  - **Understand system needs**
  - **Recommend Optimal solution**
  - **Provide IP or custom design skills to supplement existing teams**
  - **Advise on physical design issues**
  - **Undertake physical Implementation**
  - **Offer project management services**
- **Other things to look out for...**
  - **Company Stability**
  - **Track Record**
  - **Financial Backing**
  - **Customer References**



# Jennic IP and Design Services

- **Intellectual Property in**
  - **Access Networks**
    - ATM SARs and other hardware coprocessors
  - **Optical Networks**
    - Physical layer Framers and high-speed Interfaces
  - **Mixed Signal Systems**
    - Radio and Industrial systems
- **Broad Base of Experienced Engineers**
  - **Digital Design (Wired & Wireless System Knowledge)**
  - **Mixed Signal and RF Design (High speed, low power and mobile communications)**
  - **Physical Implementation (Experience down to 110nm)**
  - **Software Engineering (Embedded Applications)**



# Outsourcing Silicon Engineering Conclusions

## ASIC Implementation

- Costly
- Time consuming
- Risky

**Depending upon market FPGA may offer interim solution**

**If not, outsourcing can provide**

- **Considered, unbiased advice**
- **IP and custom design skills**
- **Expertise to realise the design**
- **Minimise risk exposure**
- **Cost effective use of funds for silicon implementation**

