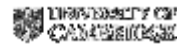


# Communication Centric Microelectronic Design

Simon Moore

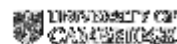
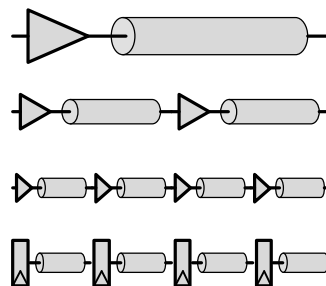
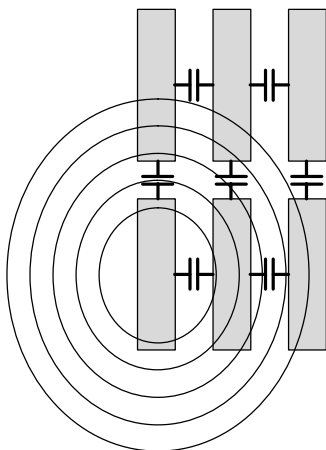
University of Cambridge  
Computer Laboratory

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## Challenges: Physical Wires

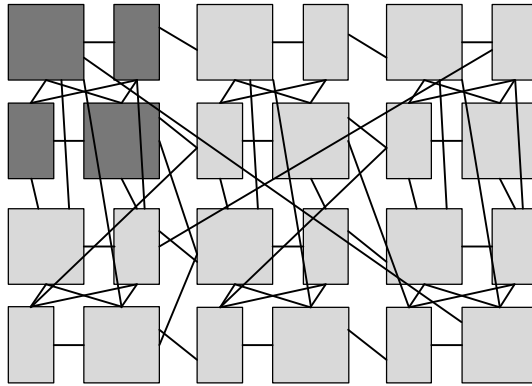
- Signal Integrity
- Speed & scaling



# Challenges: Architectural

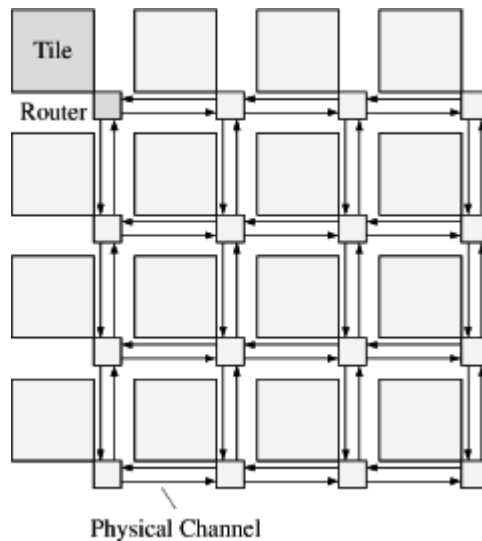
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- Wires delays result in arrays of connected blocks
- Rent's rule: exponential increase in interconnect

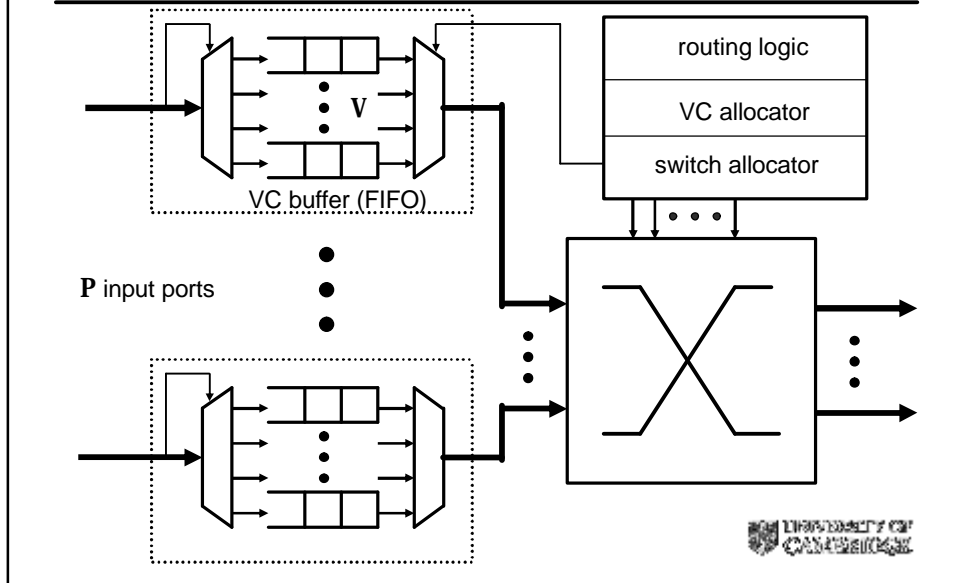


# Our Solution: Networks on Chip

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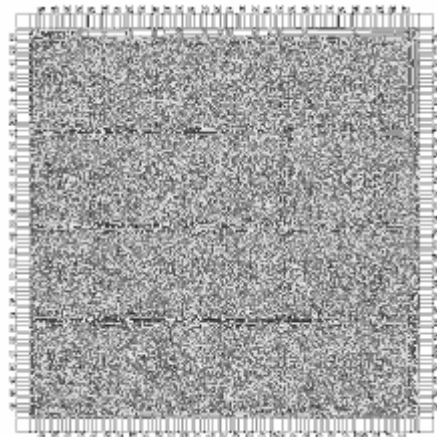


# Our Router Architecture



# Lockside test chip

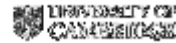
- UMC 180nm process
- 5mm x 5mm
- 4x4 network, 82-bit channels (64 data + control)
- ~5M transistors
- Mixed standard cell/ custom tool flow
- On-Chip Traffic Generation



# Future Work

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- Communication Centric Microelectronic Design
  - Explore dynamic routing of data on chip
    - Bus replacements
    - Automatic wire reuse in ASIC flows
  - ECAD tool flows
    - Exploiting channel communication
      - appearing in languages like SystemVerilog, etc.
  - Architectural challenges
    - New processor and system architectures



# Taxonomy of networks on chip

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?

Fully dynamic scheduling of wires with buffering (Lochside)

?

?

Dynamic switching with static scheduling (e.g. MIT RAW project)

?

?

Static wires

